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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/524,087	02/09/2005	Mutsumi Kikuchi	101460.55904US	2394

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EXAMINER

WELLS, KENNETH B

ART UNIT	PAPER NUMBER
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2816

DATE MAILED: 09/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/524,087	KIKUCHI ET AL.	
	Examiner	Art Unit	
	Kenneth B. Wells	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 February 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-35 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 18-35 is/are allowed.
- 6) ☒ Claim(s) 1-5, 7-9 and 11-16 is/are rejected.
- 7) ☒ Claim(s) 6, 10 and 17 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>2/9/05, 10/24/05</u> | 6) <input type="checkbox"/> Other: _____ |

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1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-5, 7-9 and 11-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamano.

As to claims 1, 11, 12, 15 and 16, note the abstract of Yamano and also Figs. 1-3, where the recited "plurality of stages of voltage booster circuits" read on circuits 6 and 7, each being used for boosting an input voltage up to a higher output voltage; the recited internal element is the memory cell which receives the pumped up output from final stage 7; and the recited details of the converter circuit 6 are shown in Fig. 2 of Yamano.

Not disclosed by Yamano is the recited voltage control means connected to the final stage circuit 7, but such would have been obvious to any person having ordinary skill in the art because such circuits are old and well-known in the art, as shown by the several references included on the attached PTO-892 form. The motivation for using such a

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circuit is to allow accurate control of the pumping circuit (as taught by each of the secondary references).

Also not disclosed by Yamano are the capacitor and diode within pump circuit 7, but this also would have been obvious to any person having ordinary skill in the art because such elements are old and well-known in the art for forming a pump circuit (of which fact official notice is taken by the examiner). The motivation for using a capacitor and diode to make pump circuit 7 is simply to utilize the most well-known pump structure to make the "black box" generic depiction of a pump.

The final limitation of claim 1 not disclosed by Yamano is the formation of the various elements on a single semiconductor substrate, but this too would have been obvious to any person having ordinary skill in the art because it is old and well-known in the art to put as much integrated circuits as possible onto a single chip (i.e., a single semiconductor die), the motivation being to form compact "single unit" IC (as opposed to requiring plural IC chips to form the circuitry of Yamano's Figs. 1-3).

As to claim 2, the same rejection as noted above with regard to claim 1 also applied to claim 1, the only difference in claim 2 being that the pump is upstream of

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the DC-DC converter, instead of downstream thereof. Such would have been obvious to any person having ordinary skill in the art because it is old and well-known in the art that a pair of series-connected elements (i.e., cascaded input-to-output) can be connected in any order, without any unexpected change in circuit operation or result. In other words, it makes no difference if the Vcc supply voltage is first pumped by DC-DC converter 6, then pumped by circuit 7, or vice-versa, the same +12V output will be obtained.

As to claims 3-5, the recited boost ratios and supply levels are deemed to be obvious design expedients to any person having ordinary skill in the art who will easily recognize that the pumping circuits of Yamano can be set to any desired values, as can the supply voltage Vcc. Thus, claims 3-5 also do not patentably distinguish over Yamano. The analysis applies for the limitations of claim 7, i.e., keeping a preset duty ratio is deemed to be well within the ordinary skill level of persons working in the art of voltage boosting circuits such as that disclosed by Yamano and claimed by applicant. The recited frequency of claim 8 is again deemed to be a routine obvious design expedient, for the same reasons noted with regard to claims 3-5.

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As to claims 9 and 14, the recited inductor structure does not define over Yamano because it is also old and well-known in the art to form inductors on IC chips in this manner.

As to claim 13, the limitation of forming the inductor wiring at the same time as forming other wiring of the circuitry shown in Figs. 103 of Yamano also would have been obvious because simultaneous formation of metal wires on an IC is also old and well-known in the art of semiconductor manufacturing (the motivation being to save both time and manufacturing steps when implementing the booster circuitry of Figs. 1-3).

2. Claims 18-35 are allowed.

Claims 6, 10 and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

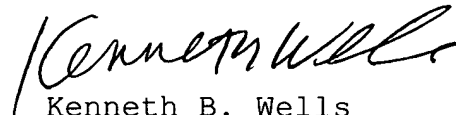
3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth B. Wells whose telephone number is (571)272-1757.

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The examiner can normally be reached on Monday through Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan, can be reached at (571)272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Kenneth B. Wells
Primary Examiner
Art Unit 2816

September 13, 2006